REMARKS

INTRODUCTION:

In accordance with the foregoing, claims 1 and 13 have been amended. No new matter is being presented, and approval and entry are respectfully requested.

Claims 1-16 are pending and under consideration. Claims 6-12 and 16 have been allowed. Reconsideration is respectfully requested.

OBJECTIONS TO THE DRAWINGS:

In the Office Action, at page 2, numbered paragraph 1, the drawings were objected to. Corrections to FIGs. 7 and 9 have been requested and replacement figures have been submitted herewith. Therefore, the outstanding drawing objections should be resolved.

Reconsideration and withdrawal of the outstanding objections to the drawings are respectfully requested.

CHANGES TO THE SPECIFICATION:

The specification has been reviewed in response to this Office Action. Changes have been made to the specification only to place it in preferred and better U.S. form for issuance and to resolve the Examiner's objections raised in the Office Action. No new matter has been added.

REJECTION UNDER 35 U.S.C. §103:

A. In the Office Action, at pages 4-8, numbered paragraph 5, claims 1, 2, and 13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Somasundaram et al. (USPN 5,491,793; hereafter Somasundaram), and further in view of Higashida (USPN 6,233,673; hereafter, Higashida). The reasons for the rejection are set forth in the Office Action and therefore not repeated. The rejection is traversed and reconsideration is requested.

It is respectfully submitted that Somasundaram discloses that a DSU outputs a serial converted instruction address to an ICE at all times (FIG. 5). Higashida discloses an ICE which removes a restriction of a number of chip terminals of an ICE CPU. However, these references do not disclose that "a data output circuit, when the branch information contains no branch, outputs a branchless signal in place of said instruction address," as is recited in amended independent claims 1 and 13.

Thus, amended claims 1 and 13 are submitted to be patentable under 35 U.S.C. §103(a) over Somasundaram et al. (USPN 5,491,793) and/or Higashida (USPN 6,233,673), alone or in combination. Since claims 2-5 depend from amended claim 1, claims 2-5 are submitted to be patentable under 35 U.S.C. §103(a) over Somasundaram et al. (USPN 5,491,793) and/or Higashida (USPN 6,233,673), alone or in combination, for at least the reasons that amended claim 1 is submitted to be patentable under 35 U.S.C. §103(a) over Somasundaram et al. (USPN 5,491,793) and/or Higashida (USPN 6,233,673), alone or in combination.

B. In the Office Action, at pages 8-11, numbered paragraph 6, claims 14 and 15 were rejected under 35 U.S.C. §103(a) as being unpatentable over Somasundaram et al. (USPN 5,491,793; hereafter, Somasundaram), in view of Higashida (USPN 6,233,673; hereafter, Higashida), as applied to claim 1 above, and further in view of Dwyer, III (USPN 6,430,682; hereafter, Dwyer). The reasons for the rejection are set forth in the Office Action and therefore not repeated. The rejection is traversed and reconsideration is requested.

It is respectfully submitted that Somasundaram fails to disclose an external in-circuit emulator, wherein the debug support unit is connected to the external in-circuit emulator via a tool bus whose bit number is smaller than said first bit number and via a bus status signal line which reports on the status of the tool bus; and wherein said debug support unit outputs said instruction address to said tool bus in series in response to an instruction fetch request signal received from said CPU, and initiates instruction-prefetch control when instruction code, which corresponds to the instruction fetch request, has been received from said in-circuit emulator, before a next instruction fetch request is received, as is recited in claim 14 of the present invention.

Although Higashida discloses an in-circuit emulator (ICE), Higashida does not disclose an external in-circuit emulator wherein the debug support unit is connected to the external in-circuit emulator via a tool bus whose bit number is smaller than said first bit number and via a bus status signal line which reports on the status of the tool bus; and wherein said debug support unit outputs said instruction address to said tool bus in series in response to an instruction fetch request signal received from said CPU, and initiates instruction-prefetch control when instruction code, which corresponds to the instruction fetch request, has been received from said in-circuit emulator, before a next instruction fetch request is received, as is recited in claim 14 of the present invention.

Although Dwyer discloses two different types of prefetching, instruction prefetching and data prefetching (col. 1, lines 17-22), Dwyer does not disclose that the debug support unit initiates instruction-prefetch control "when instruction code, which corresponds to the instruction fetch request, has been received from said in-circuit emulator, before a next instruction fetch request is received," as is described in claim 14 of the present invention.

Thus, claim 14 is submitted to be patentable under 35 U.S.C. §103(a) over Somasundaram et al. (USPN 5,491,793) and/or Higashida (USPN 6,233,673) and/or Dwyer, III (USPN 6,430,682), alone or in combination. Since claim 15 depends from claim 14, claim 15 is submitted to be patentable under 35 U.S.C. §103(a) over Somasundaram et al. (USPN 5,491,793) and/or Higashida (USPN 6,233,673) and/or Dwyer, III (USPN 6,430,682), alone or in combination, for at least the reasons that claim 14 is submitted to be patentable under 35 U.S.C. §103(a) over Somasundaram et al. (USPN 5,491,793) and/or Higashida (USPN 6,233,673) and/or Dwyer, III (USPN 6,430,682), alone or in combination.

ALLOWABLE SUBJECT MATTER:

A. In the Office Action, at page 11, paragraph 7, claims 6-12 and 16 were allowed.

B. In the Office Action, at page 12, paragraph 9, claims 3, 4 and 5 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As noted above, since claims 3-5 depend from amended claim 1, which is submitted to be allowable, claims 3-5 are submitted to be allowable for at least the reasons that amended claim 1 is submitted to be allowable.

CONCLUSION:

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot, and further, that all pending claims patentably distinguish over the prior art. Thus, there being no further outstanding objections or rejections, the application is submitted as being in condition for allowance which action is earnestly solicited.

If the Examiner has any remaining issues to be addressed, it is believed that prosecution can be expedited by the Examiner contacting the undersigned attorney for a telephone interview to discuss resolution of such issues.

If there are any underpayments or overpayments of fees associated with the filing of this Amendment, please charge and/or credit the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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IN THE DRAWINGS:

The attached drawings include changes to FIGs. 7 and 9. The sheet containing FIG. 7 replaces the original sheet including FIG. 7. In FIG. 7, in elements P20, P22, and P26, the spelling has been amended to correct the misspelling of "instruction". The sheet containing FIG. 9 replaces the original sheet including FIG. 9. In FIG. 9, in element P44, the spelling has been amended to correct the misspelling of "instruction".

Approval of these changes to the Drawings is respectfully requested.